

产品规格书

PRODUCT SPECIFICATION

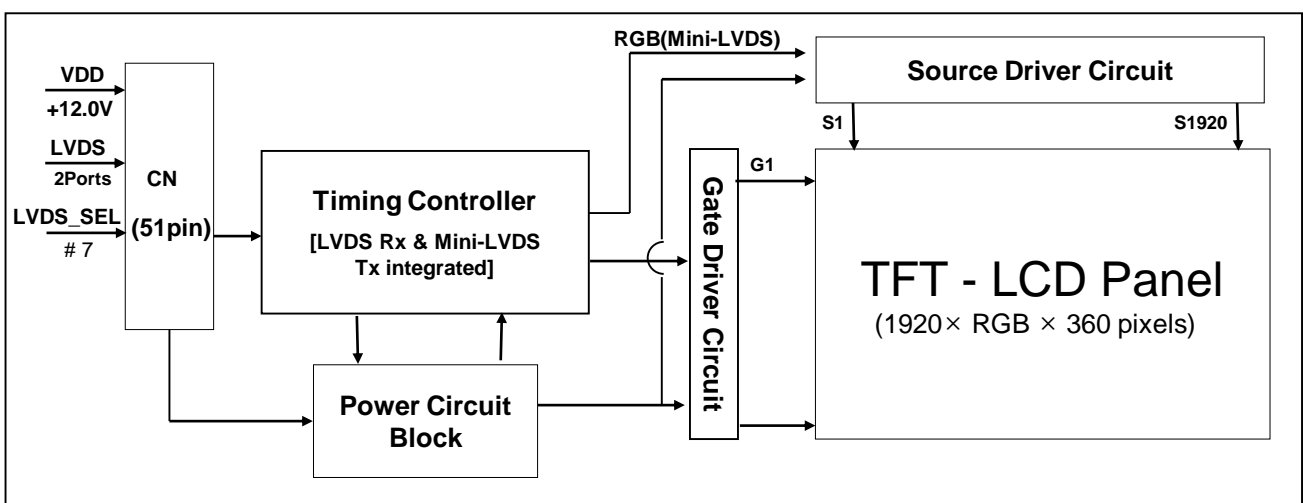
| | | | |
|---|---------------|--------------|---------------|
| 产品名称 (Model Name) <u>37.7液晶显示屏</u> | | | |
| 产品型号 (Part Number) <u>H377HDL</u> | | | |
| 项目 (Item) | 拟制 (Prepared) | 审核 (Checked) | 批准 (Approved) |
| 签名 (Signature) | | | |
| 日期 (Date) | | | |
| 备注 (Note) | | | |
| 客户 (Customer): 签名 (Signature): 日期 (Date): | | | |

| 版本介绍 (Version is introduced) | | | | |
|------------------------------|------------------------|---------------------------|---------------------------|--------------|
| 版本 (Version) | 发行日期 (Release date) | 原版描述 (Old description) | 更新描述 (New description) | 页码 (Page) |
| V.0 | 2018/12/10 | 首版 | | / |
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1.0 GENERAL DESCRIPTION

1.1 Introduction

HT377HDL-500 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This open cell has a 37.7 inch diagonally measured active area with FHD resolutions (1920 horizontal by 360 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this open cell can display 16.7M colors. The TFT-LCD panel used for this open cell is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADSDS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- High Definition TV(FHD TV)
- AV application Products

1.4 General Specification

< Table 1. General Specifications >

| Parameter | Specification | Unit | Remark |
|-------------------------|---|--------|------------------------------|
| Active area | 941.18(H) × 176.47(V) | mm | |
| Number of pixels | 1920(H) × 360(V) | pixels | |
| Pixel pitch | 0.49005(H) × RGB × 0.49005(V) | | |
| Pixel arrangement | Pixels RGB Vertical stripe | | |
| Display colors | 16.7M(8bits-true) | colors | |
| Brightness | 500cd type | | |
| Open Cell Transmittance | 5.0 (typ.) | % | At center point with BOE BLU |
| Weight | 8000 | gram | |
| Power Consumption | 80 | Watt | |
| Surface Treatment | Haze 1% , 3H, Anti-Glare Layer(for Front) , Clear(for Rear) | | |

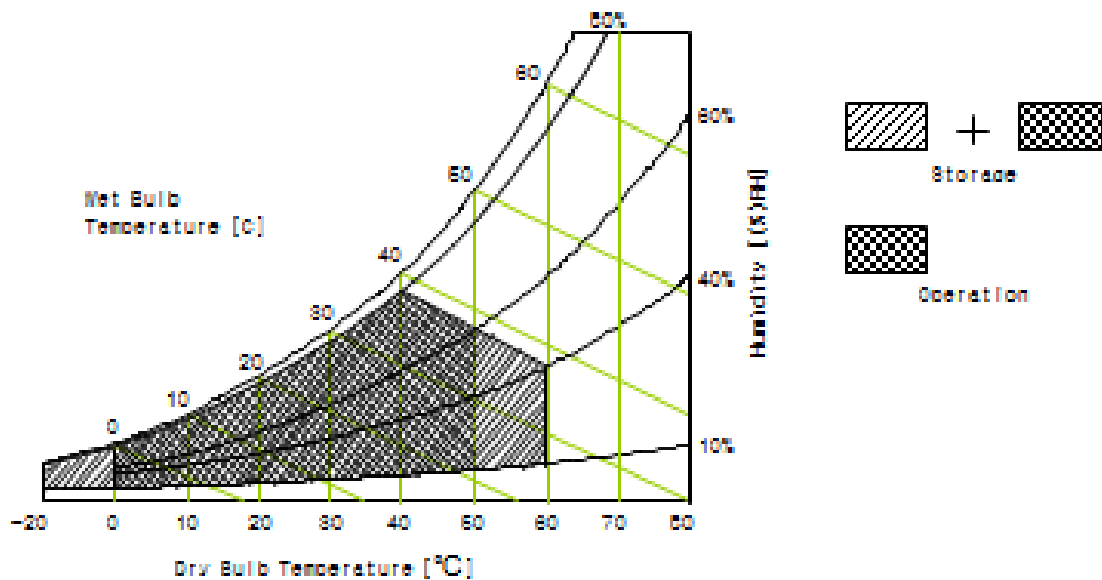
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications > [VSS=GND=0V]

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|----------------------------|------------------|---------|------|------|------------|
| Power Supply Voltage | VDD | VSS-0.3 | 14 | V | Ta = 25 °C |
| Operating Temperature | T _{OP} | 0 | +50 | °C | Note 1 |
| | T _{SUR} | 0 | +60 | °C | |
| Storage Temperature | T _{ST} | -20 | +60 | °C | |
| Operating Ambient Humidity | Hop | 10 | 80 | %RH | |
| Storage Humidity | Hst | 10 | 80 | %RH | |

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25 ± 2 °C]

| Parameter | | Symbol | Values | | | Unit | Remark |
|-----------------------------|------------------------------|--------|--------|-----|------|------|--------|
| | | | Min | Typ | Max | | |
| Power Supply Input Voltage | | VDD | 10.8 | 12 | 14 | Vdc | |
| Power Supply Ripple Voltage | | VRP | | | 300 | mV | |
| Power Supply Current | | IDD | - | 333 | 630 | mA | Note 1 |
| Power Consumption | | PDD | | 4.0 | 7.6 | Watt | |
| Rush current | | IRUSH | - | - | 3.3 | A | Note 2 |
| LVDS Interface | LVDS Swing Voltage | VID | ±100 | | ±300 | mV | Note 3 |
| | Common Input Voltage | VLVC | 1.0 | 1.2 | 1.4 | V | |
| CMOS Interface | Input High Threshold Voltage | VIH | 2.7 | - | 3.3 | V | |
| | Input Low Threshold Voltage | VIL | 0 | - | 0.6 | V | |

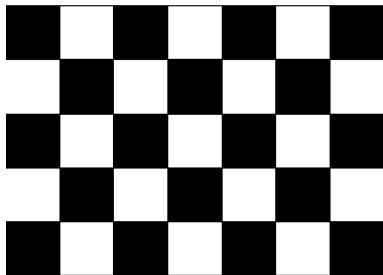
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=12.0V,

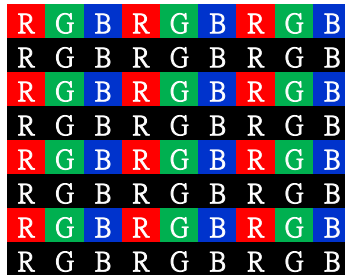
Frame rate $f_v=60\text{Hz}$ and Clock frequency = 75.4MHz.

Test Pattern of power supply current

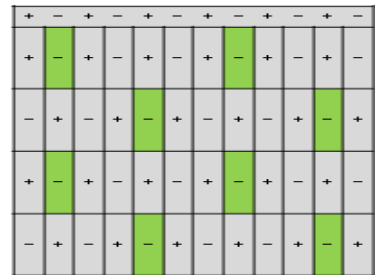
a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Horizontal 1 Line (L0/L255)



c) Flicker Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

Note 3 : The LVDS test point is at each terminal resistor

4.0 INTERFACE CONNECTION

4.1 Module Input Signal & Power

- Connector : IS050-C51B-C39-S (UJU) / FI-RE51S-HF-R1500 (JAE) or Equivalent.

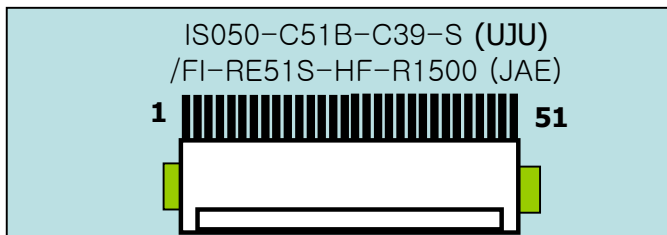
< Table 4. Open Cell Input Connector Pin Configuration >

| Pin No | Symbol | Description | Pin No | Symbol | Description |
|--------|---------|--|--------|-----------|---|
| 1 | NC | No Connection | 21 | GND | Ground |
| 2 | SDA | I ² C Data | 22 | CH1[3]- | First pixel negative LVDS differential data input. Pair3 |
| 3 | SCL | I ² C Clock | 23 | CH1[3]+ | First pixel positive LVDS differential data input. Pair3 |
| 4 | NC | Not Connected | 24 | NC | Not Connected |
| 5 | NC | Not Connected | 25 | NC | Not Connected |
| 6 | NC | Not Connected | 26 | NC or GND | Not Connected |
| 7 | SELLVDS | High: JEIDA Low or Open: VESA | 27 | NC | Not Connected |
| 8 | NC | Not Connected | 28 | CH2[0]- | Second pixel negative LVDS differential data input. Pair0 |
| 9 | NC | Not Connected | 29 | CH2[0]+ | Second pixel positive LVDS differential data input. Pair0 |
| 10 | NC | Not Connected | 30 | CH2[1]- | Second pixel negative LVDS differential data input. Pair1 |
| 11 | GND | Ground | 31 | CH2[1]+ | Second pixel positive LVDS differential data input. Pair1 |
| 12 | CH1[0]- | First pixel negative LVDS differential data input. Pair0 | 32 | CH2[2]- | Second pixel negative LVDS differential data input. Pair2 |
| 13 | CH1[0]+ | First pixel positive LVDS differential data input. Pair0 | 33 | CH2[2]+ | Second pixel positive LVDS differential data input. Pair2 |
| 14 | CH1[1]- | First pixel negative LVDS differential data input. Pair1 | 34 | GND | Ground |
| 15 | CH1[1]+ | First pixel positive LVDS differential data input. Pair1 | 35 | CH2CLK- | Second pixel negative LVDS clock |
| 16 | CH1[2]- | First pixel negative LVDS differential data input. Pair2 | 36 | CH2CLK+ | Second pixel positive LVDS clock |
| 17 | CH1[2]+ | First pixel positive LVDS differential data input. Pair2 | 37 | GND | Ground |
| 18 | GND | Ground | 38 | CH2[3]- | Second pixel negative LVDS differential data input. Pair3 |
| 19 | CH1CLK- | First pixel negative LVDS clock | 39 | CH2[3]+ | Second pixel positive LVDS differential data input. Pair3 |
| 20 | CH1CLK+ | First pixel positive LVDS clock | | | |

| Pin No | Symbol | Description | Pin No | Symbol | Description |
|--------|-----------|---------------|--------|--------|--------------------|
| 40 | NC | Not Connected | 46 | GND | Ground |
| 41 | NC | Not Connected | 47 | NC | Not Connected |
| 42 | NC or GND | Not Connected | 48 | VCC | Input Voltage +12V |
| 43 | NC or GND | Not Connected | 49 | VCC | Input Voltage +12V |
| 44 | NC or GND | Ground | 50 | VCC | Input Voltage +12V |
| 45 | GND | Ground | 51 | VCC | Input Voltage +12V |

- Notes :
1. NC(Not Connected) : This pins are only used for BOE internal operations.
 2. Input Level of LVDS signal is based on the IEA 664 Standard.
 3. LVDS_SEL : This pin is used for selecting LVDS signal data format.
 If this Pin : High (3.3V) → JEIDA LVDS format
 Otherwise : Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM



BIST Pattern

| PT1: Black (1 sec) | PT1: White (1 sec) | PT1: Red (1 sec) | PT1: Green (1 sec) | PT1: Blue (1 sec) |
|-----------------------|-----------------------|---------------------|-----------------------|----------------------|
| | | | | |

5.0 SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Table 5. Timing Table >

| Item | | Symbols | Min | Typ | Max | Unit | |
|--------------------------------|-----------|---------|-----------------|--------------|------|-------|------------------|
| Clock | Frequency | 1/Tc | 58 | 74.25 (92.8) | 97 | MHz | |
| | High Time | Tch | - | 4/7Tc | - | | |
| | Low Time | Tcl | - | 4/7Tc | - | | |
| Frame Period | | Tv | 1100 | 1125 | 1149 | lines | |
| | | | 47 | 60 (75) | 78 | Hz | |
| Horizontal Active Display Term | | Valid | t _{HV} | - | 960 | - | t _{CLK} |
| | | Total | t _{HP} | 1060 | 1100 | 1200 | t _{CLK} |
| Vertical Active Display Term | | Valid | t _{VV} | - | 360 | - | t _{HP} |
| | | Total | t _{VP} | 1100 | 1125 | 1149 | t _{HP} |

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

< Table 6. LVDS Input SSCG >

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------------------|---|--|----------------|-----------------|---------------|------|
| F | LVDS Input frequency | - | 58 | 74.25 (92.8) | 97 | MHz |
| T _{LVSK} | LVDS channel to channel skew | F=100MHz V _{IC} =1.2V V _{ID} =±200mV | -(1/F)* 30% | - | (1/F)*3 0% | ps |
| F _{LVMOD} | Modulating frequency of input clock during SSC | F=85MHz | 0 | - | 200 | KHz |
| F _{LVDEV} | Maximum deviation of input clock frequency during SSC | V _{IC} =1.2V V _{ID} =±200mV | -3 | - | +3 | % |
| T _{CY-CY} | Cycle to Cycle jitter | | - | - | 50 | ps |

5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 7. Input Signal and Display Color Table >

| Color & Gray Scale | | Input Data Signal | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----------|-------------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|
| | | Red Data | | | | | | | | Green Data | | | | | | | | Blue Data | | | | | | | |
| | | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Gray Scale of Red | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | ↑ | | | | | | | | ↑ | | | | | | | | ↑ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | ▽ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Gray Scale of Green | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | ↑ | | | | | | | | ↑ | | | | | | | | ↑ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | ▽ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Gray Scale of Blue | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| | △ | ↑ | | | | | | | | ↑ | | | | | | | | ↑ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | ▽ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| Gray Scale of White | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| | △ | ↑ | | | | | | | | ↑ | | | | | | | | ↑ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | |
| | ▽ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 8. Sequence Table >

| Parameter | Values | | | Units |
|-----------|--------|-----|-----|-------|
| | Min | Typ | Max | |
| T1 | 0.5 | - | 20 | ms |
| T2 | 10 | - | - | ms |
| T3 | 200 | - | - | ms |
| T4 | 100 | - | - | ms |
| T5 | 0 | - | - | ms |
| T6 | 1 | - | - | s |

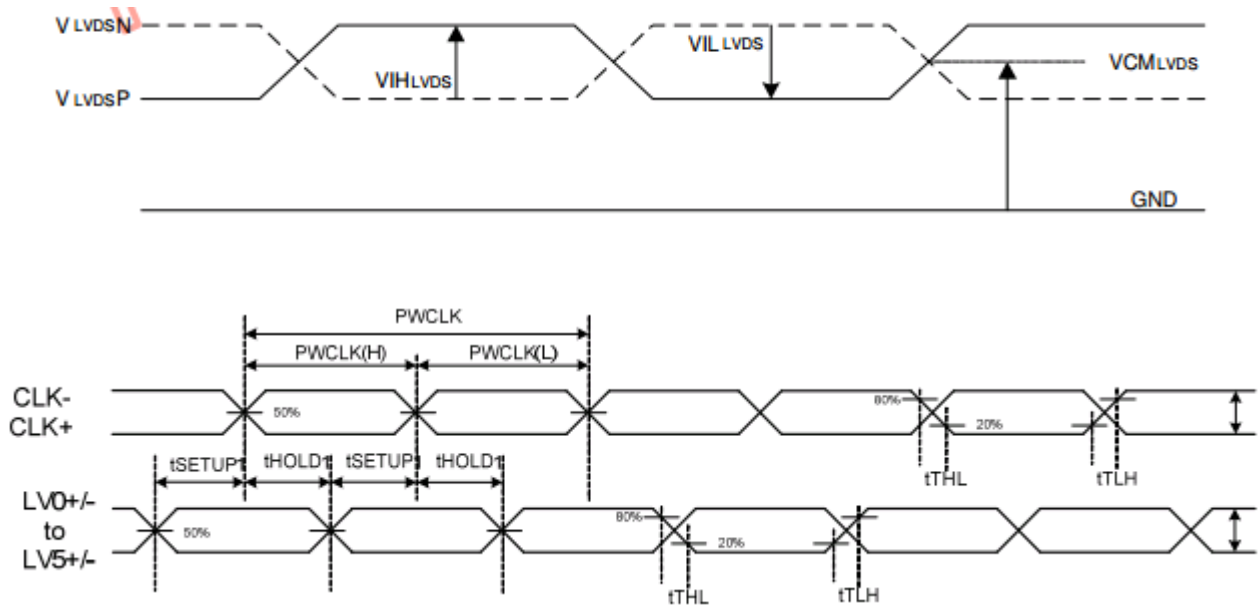
Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.

2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.

6.0 MINI-LVDS SIGNAL SPECIFICATIONS

< Table 9. Timing Table >

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|---|-----|-----|------|------|
| F_M | Mini-LVDS Clock frequency | - | - | 400 | MHz |
| F_{MLVMOD} | Modulating frequency of input clock during SSC | - | - | 600 | KHz |
| F_{MLVDEV} | Maximum deviation of input clock frequency during SSC | -3 | - | +3 | % |
| $V_{IH_{LVDS}}$ | Mini-LVDS high input voltage | 200 | - | - | mV |
| $V_{IL_{LVDS}}$ | Mini-LVDS high input voltage | - | - | -200 | mV |
| tSETUP | Data setup time | 0.5 | - | - | ns |
| tHOLD | Data hold time | 0.5 | - | - | ns |



8 前框图纸:

